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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/827,970	04/06/2001	Alasdair Rawsthorne		5419

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EXAMINER	
PHAN, THAI Q	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 04/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/827,970	RAWSTHORNE ET AL.	
	Examiner	Art Unit	
	Thai Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/27/2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicants' amendment filed on 12/27/2005. Claims 1-15 are pending in the action.

Drawings

The replacement drawing of Fig. 4 submitted on 12/27/2005 is objected to because it introduces a new matter. The drawing replacement will not be entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al, US patent no. 6,199,152 B1 in view of Le, US patent no. 6,631514.

As per claim 1, Kelly discloses a method and system for processing and protecting memory for a computer processor during normal and emulation operation with feature limitations very similar to the claimed invention. According to Kelly, the memory processing method includes steps

Mapping target register representing a working register of a subject machine for exception emulation to move data to either a first location or to a second location within

a target machine (col. 15, lines 26-46, col. 16, lines 20-40, col. 23, line 1-11, col. 32, lines 40-64, for example),

Mapping of the working register subject to exception handling between the first and second locations for code translation/conversion for exception emulation. Kelly does not expressly disclose mappings registers in alternative manner as claimed. Such claimed feature is however well-known in the art. In fact, Le teaches virtual registers including a plurality of abstract registers for mapping the registers such that one of the first or second locations represents a definitive version of the abstract register for the emulator during exception handling, while the other of the register represents a speculative version of the abstract register as claimed (col. 6, line 44 to col. 7, line 7, cols. 8-10) for handling exception and exception emulation. Le further teaches transferring or mapping legacy ISA register values to the architecture register, and reverting back to the legacy register to handle exception occur or legacy-native register mapping to handle exception occur or speculative to occur (col. 6, line 44 to col. 7, line 7, for example) in an alternative manner to handle and complete the exception occurrence as claimed.

This would motivate practitioner in the art at the time of the invention was made to combine Le teaching of virtual register mapping in a manner above into Kelly disclosure to handle and manage exceptions in a different and more efficient way on any target architecture as taught in Le.

As per claim 2, Le discloses for a predetermined section or set of instruction codes, locations holding a content or a definitive value of the abstract register, while the

other of locations holds a speculative for handling exception during code conversion or emulation as claimed.

As per claim 3, Kelly and Le disclose code conversion and code optimization including the limitations as claimed for target emulation.

As per claim 4, Kelly discloses register mapping for predetermined section of subject code as claimed (col. 13, lines 39-61, col. 16, lines 20-40, for example).

As per claim 5, Le teaches a plurality of abstract registers for selected target locations as above.

As per claims 6-8, Kelly discloses the claimed limitation during code translation for handling code exception.

As per claim 9, Kelly discloses a method for use in handling exceptions by an emulator performing program code conversion between subject code suitable for a first type (subject) processor and target code suitable for a target processor with feature limitations very similar to the claimed invention. According to Kelly, the method for code conversion in the target emulation includes steps

Providing a plurality of registers of the first type processor (Fig. 4),

Mapping the target register representing a working register of a subject machine for emulation to either a first location or to a second location within a target machine (col. 15, lines 26-46, col. 16, lines 20-40, col. 23, line 1-11, col. 32, lines 40-64, for example),

Mapping of the working register between the first and second locations for code translation/conversion for exception emulation. Kelly does not expressly disclose

mappings registers in alternative manner as claimed. Such claimed feature is however well-known in the art. In fact, Le teaches virtual registers including a plurality of abstract registers for mapping the registers such that one of the first or second locations represents a definitive version of the abstract register for the emulator during exception handling, while the other of the register represents a speculative version of the abstract register as claimed (col. 6, line 44 to col. 7, line 7, cols. 8-10) for handling exception and exception emulation.

This would motivate practitioner in the art at the time of the invention was made to combine Le teaching of virtual register mapping in a manner above into Kelly disclosure to handle and manage exceptions in a different and more efficient way on any target architecture as taught in Le.

As per claim 10, Kelly and Le disclose for a predetermined section or set of instruction codes, locations holding a content or a definitive value of the abstract register, while the other of locations holds a speculative for handling exception during code conversion or emulation, and the mapping is performed upon reaching the end of the predetermined subject code as claimed.

As per claim 11, Kelly and Le disclose a code conversion including the limitations as claimed for target emulation.

As per claims 12-13 and 14-15, Kelly discloses an emulator and computer program product for use in handling exceptions by an emulator performing program code conversion between subject code suitable for a first type (subject) processor and target code suitable for a target processor with feature limitations very similar to the

claimed invention. According to Kelly, the emulator with program product includes means for performing steps

Providing a plurality of registers of the first type processor (Fig. 4),

Mapping target register representing a working register of a subject machine for emulation to either a first location or to a second location within a target machine (col. 15, lines 26-46, col. 16, lines 20-40, col. 23, line 1-11, col. 32, lines 40-64, for example),

Mapping of the working register between the first and second locations for code translation/conversion for exception emulation. Kelly does not expressly disclose mappings registers in alternative manner as claimed. Such claimed feature is however well-known in the art. In fact, Le teaches virtual registers including a plurality of abstract registers for mapping the registers such that one of the first or second locations represents a definitive version of the abstract register for the emulator during exception handling, while the other of the register represents a speculative version of the abstract register as claimed (col. 6, line 44 to col. 7, line 7, cols. 8-10) for handling exception and exception emulation. Le further teaches transferring or mapping legacy ISA register values to the architecture register, and reverting back to the legacy register to handle exception occur or legacy-native register mapping to handle exception occur or speculative to occur (col. 6, line 44 to col. 7, line 7, for example) in an alternative manner to handle and complete the exception occur as claimed.

This would motivate practitioner in the art at the time of the invention was made to combine Le teaching of virtual register mapping in a manner above into Kelly

disclosure to handle and manage exceptions in a different and more efficient way on any target architecture as taught in Le.

Response to Arguments

In response to applicants' argument the prior art of record fails to disclose register mapping for holding a definitive or a speculative version in an alternative way as claimed, the examiner responds such argued feature is well defined in the cited references. Le teaches transferring or mapping a legacy ISA register value to the architecture register, and reverting back to the legacy register to handle exception occur or legacy-native register mapping to handle exception occur or speculative to occur (col. 6, line 44 to col. 7, line 7, for example) in an alternative manner to handle and complete exception as claimed.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 4,589,097, issued to Auslander et al, on May 1986
2. US patent no. 5,682,492, issued to McFarland et al, on Oct. 1997
3. US patent no. 5,794,029, issued to Babaian et al, on Aug. 1998
4. US patent no. 5,835,748, issued to Orenstein et al, on Nov. 1998
5. US patent no. 6,681,238, issued to Brice et al, on Jan. 2004
6. US patent no. 6,760,888, issued to Killian et al, on July 2004

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Thai Phan whose telephone number is (571) 272-3783.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Apr. 04, 2006

Thai Phan
Patent Examiner